Notice of Allowability	Application No.	Applicant(s)	
	09/824,751	KOIKE, HIROKI	
	Examiner	Art Unit	
	Esaw T Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the RCE filed 10/29/04*.

2. ☒ The allowed claim(s) is/are *1-13*.

3. ☒ The drawings filed on *03 August 2001* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 10/29/04
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Information Disclosure Statement

1. The applicant's IDS of (10/29/04) have been entered. The examiner considers the IDS.

Examiners response to the RCE

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 10/29/04 has been entered.

Examiner's statement for reason for allowance

The following is an examiner's statement for allowance:

3. Claims **1-13** have been allowed.

As per claim **1:**

The prior art (Non patent literature document, Byung-Gil Jeon et al., "a novel cell charge evaluation scheme and rest method for 4Mb nonvolatile ferroelectric RAM") of record figure 1 teach a 4Mb memory divided into blocks wherein one block is composed of 16 sections and 1 redundancy section, each 512 rows and 64 columns is chosen as a unit section size. Further, the memory plays a role as the bit-line reference voltage generator during cell charge evaluation operation (see page 281, paragraph 4). Byung-Gil Jeon et al. in "A 0.4 mu, 3.3 V 1 TIC 4 Mb

nonvolatile ferroelectric RAM with fixed bit-line reference voltage scheme and data protection circuit" of non-literature document teach a fixed bit-line reference voltage generator (FBRVG) approach illustrated in figure 1 and the FBRVG scheme provides a cell charge evaluation mode, and measure cell charge distributions for data 0 and 1 across the entire 4-MB cell population and further varying the external voltage during charge evaluation mode can easily change the reference bit-line voltage (see page 1691, paragraph 3). However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious a reference signal generator part for generating a reference signal when amplifying a data signal occurring on the bit-line, an amplifier for amplifying the data signal occurring on the bit-line when comparing it with the reference signal and a reference potential setup circuit for setting up a potential assigned from outside of said semiconductor memory device as a potential of the reference signal. Consequently, claim 1 is allowed over the prior art.

Claims 2, 4 and 11, which are directly or indirectly dependents of claim 1 are also allowable over the prior art of record.

As per claim 3:

The prior art (Non patent literature document, Byung-Gil Jeon et al., a novel cell charge evaluation scheme and rest method for 4Mb nonvolatile ferroelectric RAM) of record figure 1 teach a 4Mb memory divided into blocks wherein one block is composed of 16 sections and 1 redundancy section, each 512 rows and 64 columns is chosen as a unit section size. Further, the memory plays a role as the bit-line reference voltage generator during cell charge evaluation operation (see page 281, paragraph 4). Byung-Gil Jeon et al. in "A 0.4 mu, 3.3 V 1 TIC 4 Mb nonvolatile ferroelectric RAM with fixed bit-line reference voltage scheme and data protection

circuit" of non-literature document a teach fixed bit-line reference voltage generator (FBRVG) approach illustrated in figure 1 and the FBRVG scheme provides a cell charge evaluation mode, and measure cell charge distributions for data 0 and 1 across the entire 4-MB cell population and further varying the external voltage during charge evaluation mode can easily change the reference bit-line voltage (see page 1691, paragraph 3). However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious a reference signal generator part for generating a reference signal when amplifying a data signal occurring on the bit-line, an amplifier for amplifying the data signal occurring on the bit-line when comparing it with the reference signal and a reference potential setup circuit for setting up comprising a reference signal control for generating a potential between a source potential and a ground potential when varying the potential in one direction, applying it to the reference potential setup circuit, and controlling the potential of the reference signal, a control for controlling an address for the semiconductor and reading a data signal from the memory cell, a determination for determining a logic value of a data signal amplified by the amplifier and a storage for storing a potential value of the reference signal when the logic value determined by the determination part inverted and a statistical process for statistically processing the value of the potential stored in the storage part wherein the reference potential setup circuit for setting up a potential assigned from outside to said semiconductor memory device as a potential of the reference signal. Consequently, claim 3 is allowed over the prior art.

As per claim 5:

The prior art (Non patent literature document, Byung-Gil Jeon et al., "a novel cell charge evaluation scheme and rest method for 4Mb nonvolatile ferroelectric RAM") of record figure 1

teach a 4Mb memory divided into blocks wherein one block is composed of 16 sections and 1 redundancy section, each 512 rows and 64 columns is chosen as a unit section size. Further, the memory plays a role as the bit-line reference voltage generator during cell charge evaluation operation (see page 281, paragraph 4). Byung-Gil Jeon et al. in "A 0.4 mu, 3.3 V 1 TIC 4 Mb nonvolatile ferroelectric RAM with fixed bit-line reference voltage scheme and data protection circuit" of non-literature document teach a fixed bit-line reference voltage generator (FBRVG) approach illustrated in figure 1 and the FBRVG scheme provides a cell charge evaluation mode, and measure cell charge distributions for data 0 and 1 across the entire 4-MB cell population and further varying the external voltage during charge evaluation mode can easily change the reference bit-line voltage (see page 1691, paragraph 3). However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious a reference signal generator part for generating a reference signal when amplifying a data signal occurring on the bit-line, an amplifier for amplifying the data signal occurring on the bit-line when comparing it with the reference signal and a reference potential setup circuit for setting up comprising a setting up a potential assigned from outside of said semiconductor memory device as a potential of the reference signal, reading out a data signal from the memory cell to the bit-line and comparing for magnitude relationship in potential, the reference signal and data signal compared by the amplifying to obtain the potential of the reference signal when the magnitude relationship inverts. Consequently, claim 5 is allowed over the prior art.

As per **claim 6:**

The prior art (Non patent literature document, Byung-Gil Jeon et al., "a novel cell charge evaluation scheme and rest method for 4Mb nonvolatile ferroelectric RAM") of record figure 1

teach a 4Mb memory divided into blocks wherein one block is composed of 16 sections and 1 redundancy section, each 512 rows and 64 columns is chosen as a unit section size. Further, the memory plays a role as the bit-line reference voltage generator during cell charge evaluation operation (see page 281, paragraph 4). Byung-Gil Jeon et al. in "A 0.4 mu, 3.3 V 1 TIC 4 Mb nonvolatile ferroelectric RAM with fixed bit-line reference voltage scheme and data protection circuit" of non-literature document teach a fixed bit-line reference voltage generator (FBRVG) approach illustrated in figure 1 and the FBRVG scheme provides a cell charge evaluation mode, and measure cell charge distributions for data 0 and 1 across the entire 4-MB cell population and further varying the external voltage during charge evaluation mode can easily change the reference bit-line voltage (see page 1691, paragraph 3). However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious a plurality of bit-lines for carrying a data signal that is output by a memory cell belonging to each column of the memory cell array and an amplifier for amplifying the data signal occurring on the bit-line and a signal hold circuit for taking and holding the data signal read out to the bit-line. Consequently, claim 6 is allowed over the prior art.

Claims 7, 9, 12 and 13, which are directly or indirectly dependents of claim 6 are also allowable over the prior art of record.

As per **claim 8:**

The prior art (Non patent literature document, Byung-Gil Jeon et al., "a novel cell charge evaluation scheme and rest method for 4Mb nonvolatile ferroelectric RAM") of record figure 1 teach a 4Mb memory divided into blocks wherein one block is composed of 16 sections and 1 redundancy section, each 512 rows and 64 columns is chosen as a unit section size. Further, the

memory plays a role as the bit-line reference voltage generator during cell charge evaluation operation (see page 281, paragraph 4). Byung-Gil Jeon et al. in "A 0.4 mu, 3.3 V 1 TIC 4 Mb nonvolatile ferroelectric RAM with fixed bit-line reference voltage scheme and data protection circuit" of non-literature document teach a fixed bit-line reference voltage generator (FBRVG) approach illustrated in figure 1 and the FBRVG scheme provides a cell charge evaluation mode, and measure cell charge distributions for data 0 and 1 across the entire 4-MB cell population and further varying the external voltage during charge evaluation mode can easily change the reference bit-line voltage (see page 1691, paragraph 3). However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious a plurality of bit-lines for carrying a data signal that is output by a memory cell belonging to each column of the memory cell array and an amplifier for amplifying the data signal occurring on the bit-line and a signal hold circuit for taking and holding the data signal read out to the bit-line comprising a first control part for controlling a series of steps for generating an address to provide it to the semiconductor memory device and reading out a data signal from the memory cell, a second control part for controlling such that the signal hold circuit takes data signal read out to the bit-line, a conversion part for A/D converting the data signal taken to the signal hold circuit, a storage part of for storing data signal A/D converted by the data conversion part and a statistical process part for statistically processing data stored in the storage part. Consequently, claim 8 is allowed over the prior art.

As per **claim 10:**

The prior art (Non patent literature document, Byung-Gil Jeon et al., "a novel cell charge evaluation scheme and rest method for 4Mb nonvolatile ferroelectric RAM") of record figure 1

teach a 4Mb memory divided into blocks wherein one block is composed of 16 sections and 1 redundancy section, each 512 rows and 64 columns is chosen as a unit section size. Further, the memory plays a role as the bit-line reference voltage generator during cell charge evaluation operation (see page 281, paragraph 4). Byung-Gil Jeon et al. in "A 0.4 mu, 3.3 V 1 TIC 4 Mb nonvolatile ferroelectric RAM with fixed bit-line reference voltage scheme and data protection circuit" of non-literature document teach a fixed bit-line reference voltage generator (FBRVG) approach illustrated in figure 1 and the FBRVG scheme provides a cell charge evaluation mode, and measure cell charge distributions for data 0 and 1 across the entire 4-MB cell population and further varying the external voltage during charge evaluation mode can easily change the reference bit-line voltage (see page 1691, paragraph 3). However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious a plurality of bit-lines for carrying a data signal that is output by a memory cell belonging to each column of the memory cell array and an amplifier for amplifying the data signal occurring on the bit-line and a signal hold circuit for taking and holding the data signal read out to the bit-line comprising reading out a data signal from the memory cell to the bit-line, taking the data signal read out to the bit-line, to the signal hold circuit and reading out the potential of data signal taken to the signal hold circuit to outside. Consequently, claim 10 is allowed over the prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for after final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Esaw Abraham

Esaw Abraham

Art unit: 2133

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